REMARKS

Applicants amended claims 15 and 19 to more precisely define the method of the present invention. Claims 15 – 22 are pending in this application. Reconsideration of the patentability of the pending claims is requested in view of the remarks and amendments set forth herein.

Applicants respectfully request that this Amendment under 37 CFR 1.116 be entered by the Examiner, placing claims 15 – 22 in condition for allowance. Applicants submit that the proposed amendments to the claims do not raise new issues or necessitate any additional search of the art. Therefore, this Amendment should be entered and considered.

Entering the Amendment would allow Applicants to reply to the 35 USC 112 rejection and place the application in condition for allowance. Alternatively, Applicants submit that entry of the Amendment would place the application in better form for appeal in the event the patentability of the pending claims is disputed.

I. 35 USC 112 , Second Paragraph Rejection

All of the proposed amendments were made to overcome the 35 USC 112 rejections. Applicants have replaced "each wafer element" with "each wafer assembly" to correct the lack of antecedent for "wafer element". In addition, Applicants have amended claim 19 to include a reference to "a wafer frame", thereby correcting the lack of antecedent in claim 22. The Office Action dated May 26, 2005 states that claims 15- 18 and 22 are indefinite for failing to particularly point out and distinctly claim.. the invention. It was stated that "in order to obtain a plurality of wafer assemblies, the step of placing must be repeated at least twice." This 112 rejection is respectfully traversed.

Applicants submit that the text of claim 15 is definite enough for the skilled artisan to understand that each wafer element has a corresponding wafer frame. Similarly, it would be understood by the skilled artisan that

"placing each wafer of said plurality of wafers on a corresponding wafer frame" will result in a plurality of wafer assemblies being obtained. It is submitted that claim 15 as amended is now sufficiently definite. Applicants therefore request the withdrawal of all of the 112 rejections of claims 15 -18 and 22.

II. Rejections Over the Prior Art

The Examiner's basis for rejecting the pending claims hinges on two assertions: 1) that the orientation of the wafer assemblies must be known at all times during processing and/or storage; and 2) that the wafer assemblies of Takeuchi should have the same orientation when being placed into the container of Kawada. However, neither Takeuchi nor Kawada suggest either assertion 1) or assertion 2). Moreover, there is no motivation to combine Takeuchi with Kawada to obtain the presently claimed invention. Assuming arguendo, that the skilled artisan would combine the teachings of Takeuchi with Kawada, the claimed invention would still not be obtained as explained below.

A. 35 USC 103 (a) Rejection over Kawada in view of Takeuchi

Claims 15 -18 stand rejected under 35 USC 103(a) over Kawada in view of Takeuchi. This rejection is traversed.

Kawada discloses a storage container for wafers that consists of slots or shelves on which each wafer is supported. It is not possible for these slots (16) to constitute orientation artifacts as suggested by the Examiner (*Office Action dated 01/14/2005 at page 2*) for at least two reasons (note paragraph 20 of the specification at page 5). In the present invention, an orientation artifact preferably has an irregular contour that mates with a corresponding alignment artifact in the wafer element. There is nothing irregular about the slots in Kawada that would function to orient the wafer elements in a desired position. In particular, the slots (16) in Kawada's containers lack the type of contour that would permit engagement with a wafer element as recited in claim 15 of the present

invention. In summary, Kawada simply lacks anything that would serve as an orientation artifact for mating with an alignment artifact on a wafer element. The result is that Kawada's container stores wafers in dissimilar and unknown orientations.

Takeuchi fails to remedy the deficiencies of Kawada. The Examiner has asserted that "the orientation of the wafer assemblies must be known at all times during processing and/or storage". This is simply not true in the prior art. It is well known that during wafer processing the orientation of each wafer assembly is unknown. Accordingly, it is typical to have a prealignment stage as illustrated by Takeuchi. In Takeuchi's process, wafer frames are taken out of a container and then taken to a prealignment section where they are sequentially aligned in the direction θ. *(See 5,238,876 patent at col. 5, lines 4-10.)*

Takeuchi discloses semiconductor wafers on a frame ring with locating portions 11a (hereinafter notch). Takeuchi's container is clearly not constructed to mate with at least one notch of a framed wafer. Indeed, Takeuchi describes a process for scribing and dividing up wafers into die. In Takeuchi's process, wafer frames are taken out of a container and then oriented in the direction θ. *(See 5,238,876 patent at col. 5, lines 4-10.)* In Applicants' invention the wafers are in a known orientation during storage, rendering it unnecessary to remove the wafers to prealign them to a known orientation during wafer processing. In addition, Takeuchi fails to teach or suggest storing a stack of wafers—such as Kawada's wafers—in a manner that would allow the orientation of the stack to be visible and known as recited in claim 15.

The Examiner states that "the wafer assemblies of Takeuchi should have the same orientation when being placed into the container of Kawada". It is unclear how Takeuchi's wafer assemblies will have the same orientation after being placed into Kawada's container. Applicant submits that there is no basis for concluding that Takeuchi's wafer elements will have the same orientation, as the notches in Takeuchi are not mated to any portion of Kawada.

B. Claims 19 -22 are also Patentable over the Cited Prior Art

Neither Kawada nor Takeuchi, nor their combination, teach or suggest specific recitations of claims 19 -22. Specifically, Kawada and Takeuchi fail to teach or suggest:

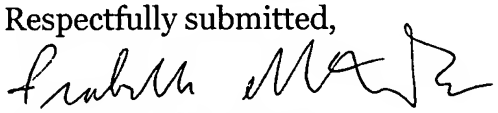
a. providing a container that conforms to the outer dimension of the wafer elements; and
b. placing the wafer elements in the container so that the alignment of each wafer element mates with at least one orientation artifact of the container.

Moreover, neither Kawada nor Takeuchi teach or suggest storing a wafer stack in a container wherein each wafer element has an orientation that is visible when the chamber is uncovered as recited in claim 20. Although the examiner asserts that it would have been obvious to place the wafer so that its notch is visible, the citation for such an assertion is not provided. Accordingly, Applicants respectfully submit that all of the new claims are patentable over the cited prior art.

III. Conclusion

Therefore, Applicants respectfully request a Notice of Allowance indicating that claims 15 - 22 are allowable. The Examiner is encouraged to contact the undersigned if any matters remain to be discussed concerning the allowance of the present application.

Respectfully submitted,



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